Amendment Under 37 C.F.R. § 1.116
Expedited Procedure – Art Unit 2823

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2507
Liming Tsau	Art Unit: 2823
Appl. No.: 10/750,834	Examiner: Khiem D. Nguyen
Filed: January 5, 2004	Atty. Docket: 1875.0230001

For: **High Density Metal Capacitor Using Via Etch Stopping Layer as Field Dielectric in Dual-Damascence Interconnect Process**

Declaration of Liming Tsau Under 37 C.F.R. § 1.131

Box AF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The undersigned, Liming Tsau, declare and state that,

1. I am the inventor of the above-captioned application, U.S. Appl. No. 10/750,834, filed January 5, 2004. I am also the inventor of U.S. Appl. No. 09/753,664, filed January 4, 2001, now U.S. Patent No. 6,803,306.

2. The '834 Application is a continuation of the '306 patent.

3. Prior to July 24, 2000, I, the inventor, had conceived of my invention in the United States, as claimed in the subject application, and diligently proceeded to file a patent application as evidenced by the attached redacted Information Disclosure Form. (Exhibit A).

4. From prior to July 24, 2000 through January 4, 2001, my Information Disclosure Form was processed in the ordinary course of business through Broadcom Corporation ("Broadcom") until it was forward to Broadcom's patent counsel, after which I worked diligently with Broadcom's patent counsel to prepare the original patent application that was filed on January 4, 2001 as Application no. 09/753,664 ("the '664 application). The filing of the '664 application constituted a constructive reduction to practice of the invention.

5. Thus, the invention was conceived prior to July 24, 2000, the filing date of Ma et al., U.S. Patent No. 6,329,234, and I, Broadcom, and Broadcom's patent counsel

worked diligently from a date prior to the filing of Ma et. al. until January 4, 2001, the filing date of the '664 application, to constructively reduce the invention to practice.

6. As the person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issue thereupon.

9/17/05
Date

Liming Tsau
Liming Tsau

BROADCOM CORPORATION

CONFIDENTIAL

Forward to:
Dee Henderson
Intellectual Property Coordinator
Ext. 5958, dhen@broadcom.com

Broadcom File No. BP 1600,

Date: ___ /

BCM Chip No. _____

INVENTION DISCLOSURE FORM

Operations

1. Title of Invention: High Density Metal Capacitor using Via Etch Stopping Layer as Field Dielectric in Dual-damascene Interconnect Process

949-585-5855

Sokol

Inventor(s) Liming Tsau
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City, State, Zip

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Citizenship

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Full Name

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Residence Address

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City, State, Zip

_____
Citizenship

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Invention Disclosure Form (*cont'd*) **CONFIDENTIAL**

2. When was the invention first conceived?_ _____

3. (a) When were first sketches, diagrams or drawings made?_ (See attached file "Copper Capacitor")_
(Append copies.)
(b) Where are they?_In the attached file_____
(c) Drawing or Notebook Ref. Nos. _____

4. (a) When was first written description made?_ _____
(Append copy.)
(b) Where is it?__In the attached file_____

5. (a) When was first explanation of invention made to others?__Not Yet_____
(b) Where?_____
(c) To whom? _____

6. (a) When was model of invention first built?_ _____
(b) Where?_____

7. (a) When was model of invention first tested or demonstrated?__Not Yet_____
(b) Where?_____
(c) Present location of model tested_____
(Append photographs.)
(d) Who witnessed such test or demonstration?_____

8. Has the invention been (a) publicly disclosed; (b) placed in commercial use; (c) offered for sale or sold; or (d) described in a printed publication? ☐ Yes X No

If "Yes," describe the first occurrence of each of (a) through (d), respectively, and give dates, places and identification.
_No._____

_____

If "no," are any of (a) through (d) contemplated? ☐ Yes X No

9. Identify known closely related publications, patents and patent applications and prior products.

_____

_____

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Invention Disclosure Form (*cont'd*) **CONFIDENTIAL**

SIGNATURES: Please sign and date. Print name below signature line.

Signature of inventors(s)

Liming Tsau — Date _____

LIMING TSAU

_____ Date _____

_____ Date _____

_____ Date _____

_____ Date _____

INSTRUCTIONS FOR SUBMISSION AND APPROVAL:

1. **Submit original to Dee Henderson**
2. **Forward one copy to Engineering Manager for approval and circulation to Engineering Director/VP and Business Unit VP/GM.**
3. **Business Unit VP/GM will forward approved copy to Dee Henderson**

ENGINEERING MANAGER APPROVAL: (required, if applicable)

Vincent Chen — Date _____

COMMENTS: _____

ENGINEERING DIRECTOR/VP APPROVAL: (required)

VAHID MANJAR — Date _____

COMMENTS: _____

BUSINESS UNIT VP/GM APPROVAL: (required)

_____ Date _____

COMMENTS: waived

On the following Invention Disclosure Sheet(s) describe the various aspects of the invention according to the following instructions:

1. **Background**: Describe the field to which invention relates, the most relevant prior art, and explain what is wrong with the prior art. Make sure to give adequate background information to enable the reader to clearly appreciate the problems that existed prior to your invention. Refer to and include relevant publications.

2. **Summary of Invention**: Briefly describe the present invention and how it solves the prior problem.

3. **Description of Invention**: Write a detailed description of the invention, referenced to sketches of the invention. If necessary, use additional sheets, and you may refer to separate drawings or photographs by number. The signature information at the bottom of this page must appear on each added sheet and on each separate drawing or photograph.

4. **Differences Over Known Prior Art**: Identify significant differences over any known prior art if possible.

5. **Advantages**: List and explain the advantages of the invention in the order of their importance.

6. **Witness**: Have two individuals, not inventors and co-inventors, read, understand, sign and date each Invention Disclosure Sheet.

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Invention Disclosur Form (*cont'd*) **CONFIDENTIAL**

INVENTION DISCLOSURE SHEET

High Density Metal Capacitor using Via Etch Stopping Layer as Field Dielectric in Dual-damascene Interconnect Process

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See the attached 12 pages

Signature of Inventor	Date
Signature of Inventor	Date
Signature of Inventor	Date

WITNESSED AND UNDERSTOOD:

Surya Bhattacharya Witness (Not an Inventor)	Date
Henry Chen Witness (Not an Inventor)	Date

High Density Metal Capacitor using Dual-damascene Copper Interconnect

Liming Tsau

Summary

•Background:

Metal-electrode Capacitors are widely used in mixed-signal/RF integrated circuits for better linearity and higher Q (due to lower electrode resistance). MiM (metal-insulator-metal) capacitors have been commercially available in the standard CMOS mixed-signal process with aluminum interconnect, by adding a few extra steps in the process flow. However, similar MiM capacitors are still been developed for the most advanced copper interconnect, which is replacing the aluminum interconnect in the 0.15um generation and beyond. Due to the uniqueness in the copper damascene process, there is no simple/low-cost way of making MiM capacitors.

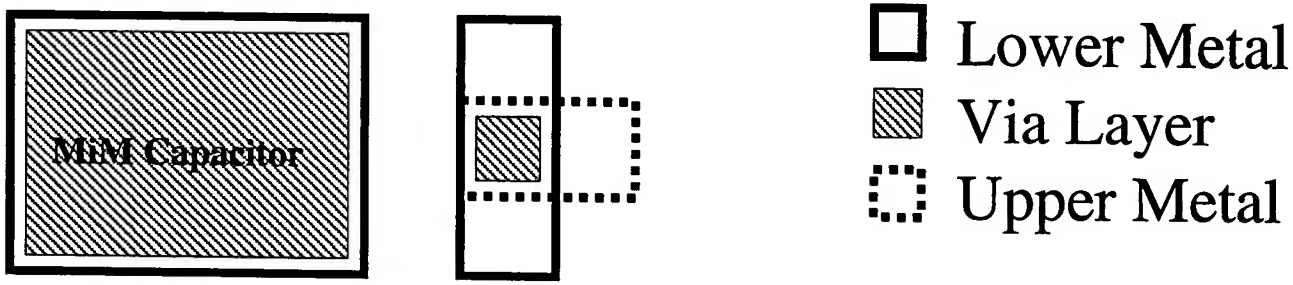
•Advantage:

The capacitors proposed in this innovation disclosure are specially designed for the copper dual-damascene process. These capacitors are fully CMOS logic process compatible. There is no extra process steps required and hence no extra cost.

Summary (Continued)

•Description of the innovation:

In a dual-damascene process, there is usually a dielectric layer on top of the metal, which is used as an etch stopping layer for the via etch. This layer is always removed in the subsequent metal trench etch. However, if one violates the design by drawing a via layer without a metal layer on top of it, this etch stopping layer can be used as the field dielectic between the bottom metal and the via layer to form a metal-insulator-metal (MiM) capacitor. A top view of the layout is illustrated in the drawing below.

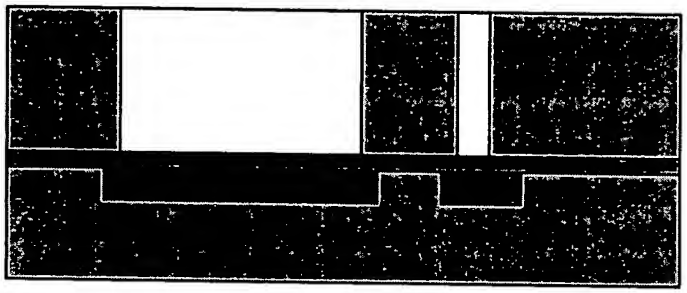


Summary (Continued)

•Technical details:

In the "via-first" dual-damascene process (which is the case in the TSMC 0.13um process), the via/metal definition is carried out in the following process steps.

(1) via photo/etch/strip: there is etch stopping layer (usually SiN) at the bottom of the via to prevent copper of the previous metal from exposure to the resist strip chemicals. The following drawing shows the cross-sectional view of the interconnect layers after the via etch and strip process.



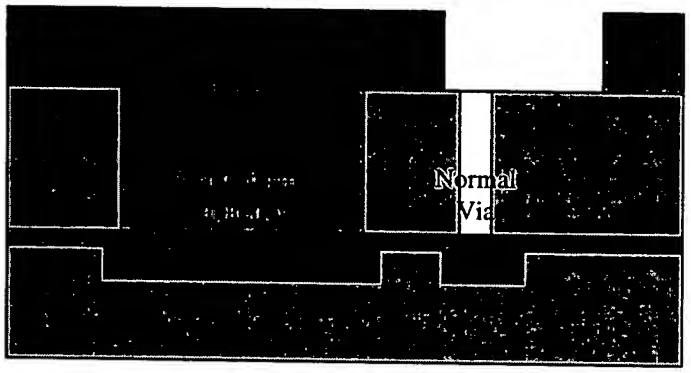
Inter-metal dielectric

SiN (etch stopping layer)

Cu (copper)

Summary (Continued)

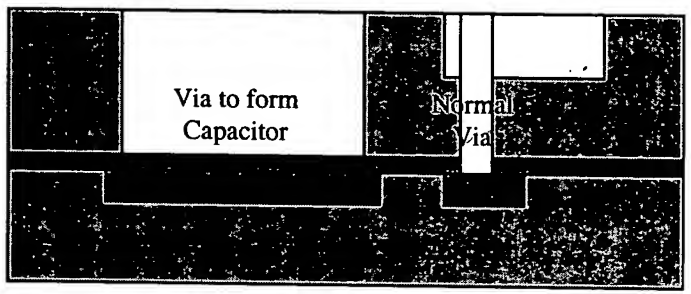
(2) metal photo: In the circuit layout, if one skips the metal layer on top of the via, the etch stopping layer will be covered by the photo resist. For other via's, there is always a metal layer on the top and the etch stopping layer will be exposed.



- Photo resist for metal etch
- Inter-metal dielectric
- SiN (etch stopping layer)
- Cu (copper)

Summary (Continued)

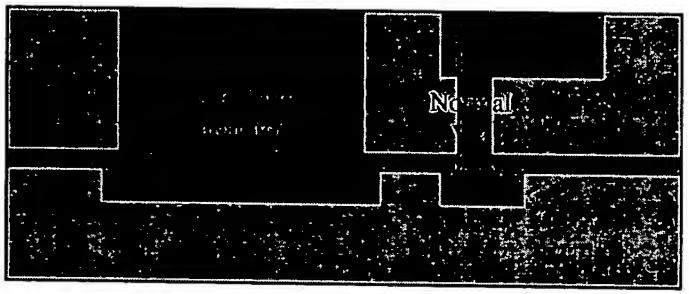
(3) metal etch/strip: the etch stopping layer at the bottom of the normal via is removed in the last step of the metal etch. However the etch stopping layer stays in the via where there is no upper metal in the layout, as shown on the left-hand side of the drawing below.



- Inter-metal dielectric
- SiN (etch stopping layer)
- Cu (copper)

Summary (Continued)

(4) metal (usually Cu) deposition and CMP: after these steps, metal (Cu) is filled in the via holes and metal trenches. As illustrated in the following drawing, a normal via is formed on the right-hand side to connect the upper metal to the lower metal and a MiM capacitor is formed on the left-hand side.



- Inter-metal dielectric
- SiN (etch stopping layer)
- Cu (copper)

Summary (Continued)

•Drawings:

In the next pages, three examples of metal capacitor using the SiN etch stopping layers as the dielectric are proposed. For simplicity, only 5 via fingers per electrode are shown in each case. In reality, the structure can be much larger for higher capacitance value. Also in each case, the entire electrode 2 is caged in electrode 1 (which is usually grounded) for noise isolation.

In the first example, the two electrodes are perpendicular to each other, which makes the absolute value of the capacitance least sensitive the photo mis-alignments.

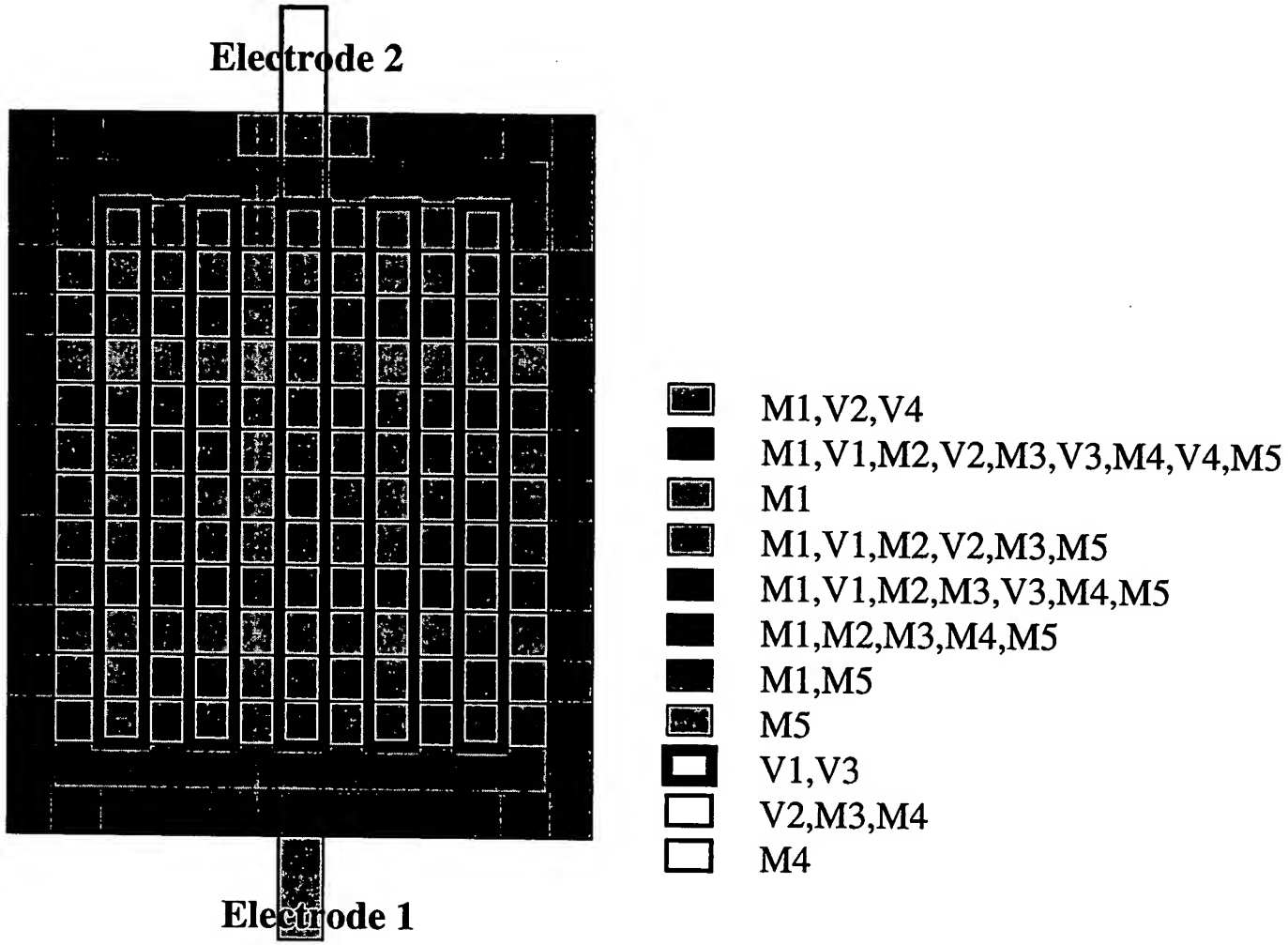
In the second example, the capacitance value is about 2X of that in the first case. It can be used when the circuit is not sensitive to the absolute value of the total capacitance (but the matching of two capacitors in the same die.)

In the third example, the capacitance value can be even larger than the second example due to the extra intra-layer metal coupling. Like the second case, this type of capacitors are sensitive to photo misalignment and can be used when the capacitance matching is critical.

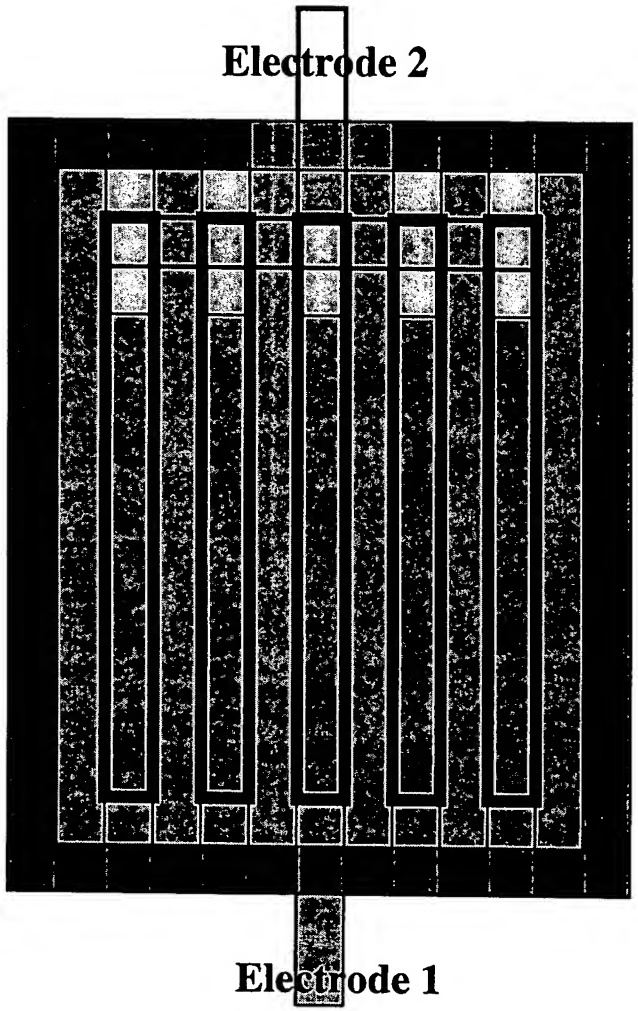
Summary (Continued)

•Importance for the company:

It is Broadcom's strength to be able to manufacture mixed-signal products by using standard CMOS logic process for lower wafer cost and shorter process time. Reduction in the capacitor area with good yield usually means reduction in the wafer cost. The invention presented in this disclosure file provides very high density capacitors for the most advanced copper interconnect process which Broadcom will be running production with in the near future.

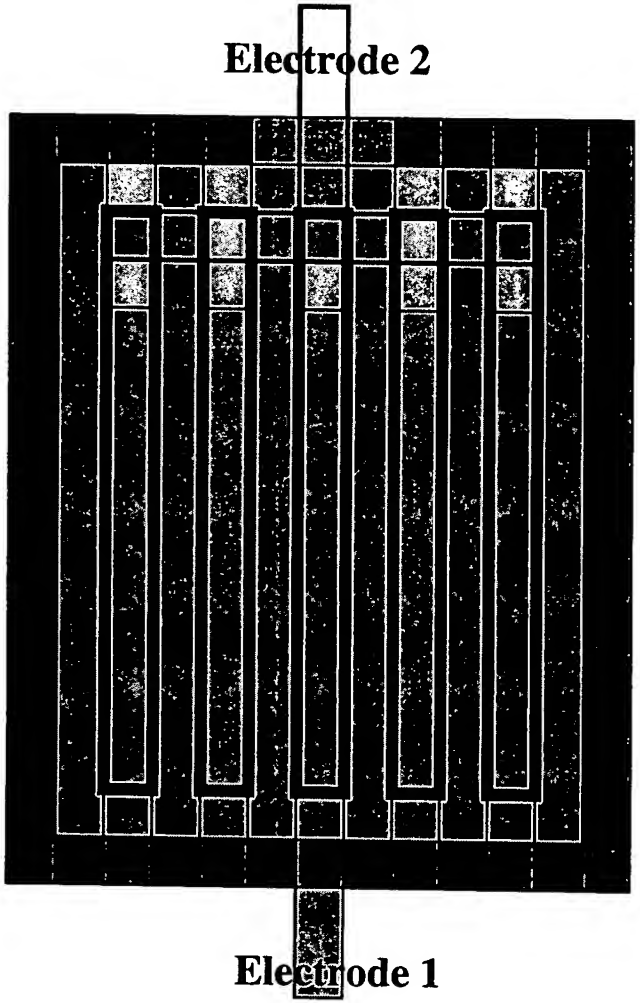

Electrode 2
Electrode 1
M1,V2,V4
M1,V1,M2,V2,M3,V3,M4,V4,M5
M1
M1,V1,M2,V2,M3,M5
M1,V1,M2,M3,V3,M4,M5
M1,M2,M3,M4,M5
M1,M5
M5
V1,V3
V2,M3,M4
M4

Case 2 All Layers



M1,V2,V4
M1,V1,M2,V2,M3,V3,M4,V4,M5
M1
M1,V1,M2,V2,M3,M5
M1,V1,M2,M3,V3,M4,M5
M1,M2,M3,M4,M5
M1,V4
M5
V1,V3
V2,M3,M4
M4

Case 3 All Layers



M1,V2,V4
M1,V1,V3,V4
M1,V1,M2,V2,M3,V3,M4,V4,M5
M1
M1,V1,M2,V2,M3,M5
M1,V1,M2,M3,V3,M4,M5
M1,M2,M3,M4,M5
M1,V4
M5
V1,V3
V2
M3,M4
M4